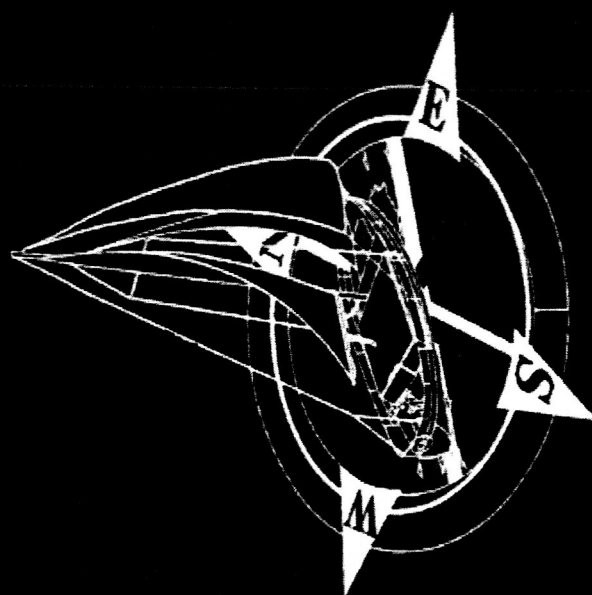




PCB Design With HDL Designer

- v **Motivation**
 - **Time savings**
 - **Money savings**
 - **Simplicity**
- v **Approach**
 - **Use single tool for PCB and FPGA design**
 - **More FPGA designs than PCB designers**
 - v **Use HDL designer for schematic capture**



PCB Design With HDL Designer Design Process

- ✓ **PCB Design Process (Minimal):**
 - **Schematic Capture**
 - **Displaying Reference Designators and Component Information on Schematic**
 - **Netlist Creation and Conversion**

PCB Design With HDL Designer

Schematic Capture - Symbols

- v **Part Symbols**

- **HDL Symbol Editor**

- v **Part Name**
 - v **Part Number**
 - v **Package Type**
 - v **Pin Name (or Port Name)**
 - v **Pin Number**

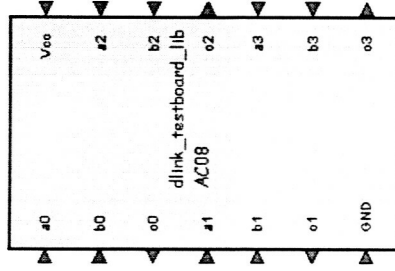
PCB Design With HDL Designer

Schematic Capture - Symbols

```
Package List
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
```

Generic Declarations

```
pin_a0 string "1"
pin_b0 string "2"
pin_a0 string "3"
pin_a1 string "4"
pin_b1 string "5"
pin_a1 string "6"
pin_gnd string "7"
pin_o3 string "8"
pin_b3 string "9"
pin_a3 string "10"
pin_o2 string "11"
pin_b2 string "12"
pin_a2 string "13"
pin_vcc string "14"
part_num string "part_ac08"
pkg_type string "dip14"
```



Declarations

```
Ports:
GND : IN
Vcc : IN
a0 : IN
a1 : IN
a2 : IN
a3 : IN
b0 : IN
b1 : IN
b2 : IN
b3 : IN
o0 : OUT
o1 : OUT
o2 : OUT
o3 : OUT
User1
```

```
std_logic
std_logic
std_logic
std_logic
std_logic
std_logic
std_logic
std_logic
std_logic
std_logic
std_logic
std_logic
std_logic
std_logic
```

<company name>		<enter comments here>	

PCB Design With HDL Designer Schematic Capture – Schematic Diagrams

√ Schematic Diagrams

—HDL Block Diagram Editor

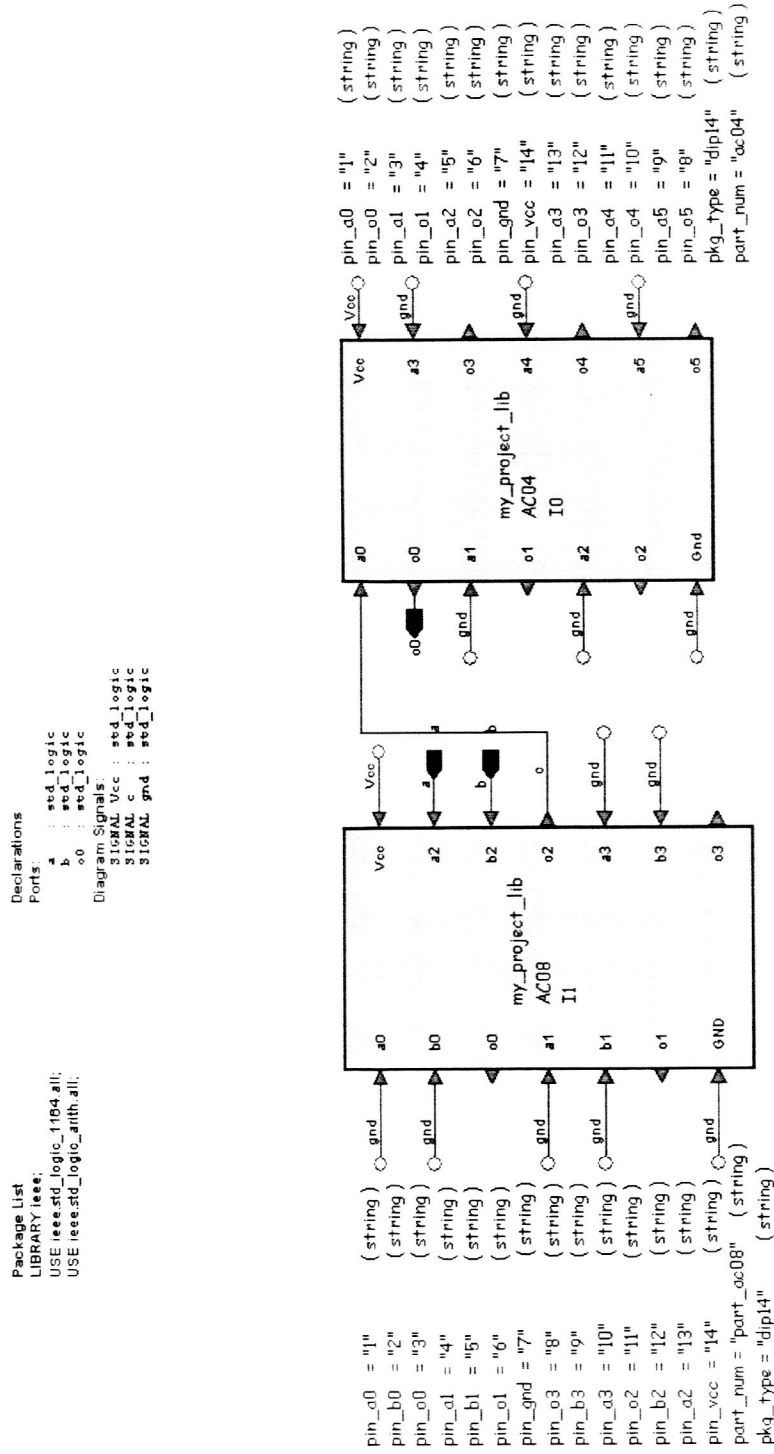
√ Part Information from Part Symbol

- √ Pin Number**
- √ Package Type**
- √ Part Number**
- √ Connection Information**
- √ Nets**
- √ Reference Designators**



PCB Design With HDL Designer

Schematic Capture – Schematic Diagrams



<tlfourcode>	test circuit

PCB Design With HDL Designer

VHDL Coding

∨ Issue – Where to include Pin Numbers in VHDL?

—Comments

∨ Possible

—VHDL Attributes

∨ Good Approach but not displayed on Block Diagrams in HDL Designer

— VHDL Generics

∨ Chosen Approach but displays pin numbers as a block of text



PCB Design with HDL Designer

Netlist Conversion

✓ Issue – How can a PADS netlist be produced?

—Comments

✓ Possible

—VHDL Attributes

✓ Good Approach but not displayed on Block Diagrams in HDL Designer

— VHDL Generics

✓ Chosen Approach but displays pin numbers as a block of text

```
GENERIC (  
    pin_a0 : string := "1";  
    pin_o0 : string := "2";  
    pin_a1 : string := "3";  
    pkg_type : string := "dip14";  
    part_num : string := "part_ac04"  
);
```



Conclusion

- ✓ Approach can be used PCB design

- Would like Vendor to study modifications to HDL Designer

- ✓ Schematic Display
 - ✓ PCB netlist output options
 - ✓ Design Rule Checking
 - ✓ Part List Generation